1. General Description

This Flash ROM-Based 8-bit micro-controller uses a fully static CMOS technology process to achieve higher speed and smaller size with the low power consumption and high noise immunity. On chip memory includes 4K words of ROM, 256 bytes of EEPROM and 192 bytes of static RAM.

2. Features

The followings are some of the features on the hardware and software:

- Fully CMOS static design
- 8-bit data bus
- On chip FLASH ROM size: 4.0 K words
- Internal RAM size: 192 bytes
- Internal EEPROM size: 256 bytes
- 37 single word instructions
- 14-bit instructions
- 8-level stacks
- Operating voltage: 2.5 V ~ 5.5 V (PEDH Disable)
  4.5 V ~ 5.5 V (PEDH Enable)
- Operating frequency: DC ~ 20 MHz
- The most fast execution time is 200 ns under 20 MHz in all single cycle instructions except the branch instruction
- Addressing modes include direct, indirect and relative addressing modes
- Power-on Reset
- Power edge-detector Reset
- Sleep Mode for power saving
- Capture, Compare, PWM module
- 7 interrupt sources:
  -External INT pin
  -TMR0 timer, TMR1 timer, TMR2 timer
  -A/D conversion completion
  -Port B<7:4> interrupt on change
  -CCP1
- A/D converter module:
  -5/7 analog inputs multiplexed into one A/D converter
  -8-bit resolution
- TMR0: 8-bit timer/counter
  TMR1: 16-bit timer/counter
  TMR2: 8-bit timer
- 5 types of oscillator can be selected by programming option:
  IRC－Internal 16MHz RC oscillator
  RC－Low cost RC oscillator
  LFXT－Low frequency crystal oscillator
  XTAL－Standard crystal oscillator
  HFXT－High frequency crystal oscillator
- On-chip RC oscillator based Watchdog Timer (WDT)
- 22/24/26/28 I/O pins with their own independent direction control

	PINS	I/O	OSC	AD CH
MDT14F201S11	28	24	IRC 16M	7
MDT14F201K11	28	24		
MDT14F201P11	32	28		
MDT14F201LQ11	32	28		

	PINS	I/O	OSC	AD CH
MDT14F201S12	28	22	HF, XT, RC, LF	5
MDT14F201K12	28	22		
MDT14F201P12	32	26		
MDT14F201LQ12	32	26		

3. Applications

The application areas of this MDT14F201 range from appliance motor control and high speed auto-motive to low power remote transmitters/receivers, pointing devices, and telecommunications processors, such as Remote controller, small instruments, chargers, toy, automobile and PC peripheral … etc.

4. Pin Assignment

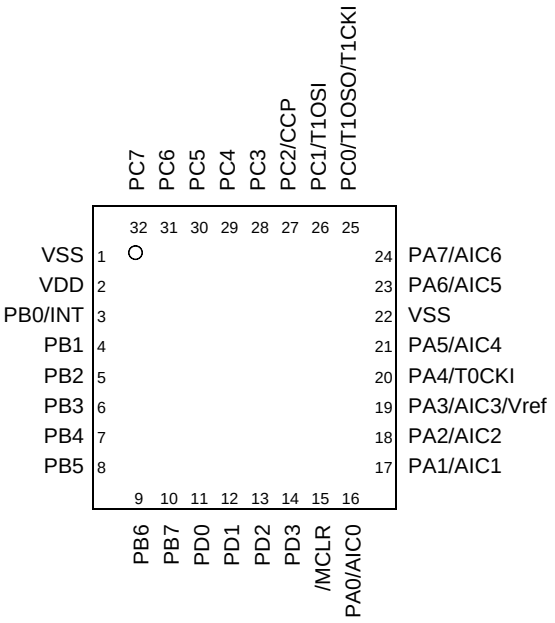
PD2	1	32	PD1
PD3	2	31	PD0
/MCLR	3	30	PB7
PA0/AIC0	4	29	PB6
PA1/AIC1	5	28	PB5
PA2/AIC2	6	27	PB4
PA3/AIC3/Vref	7	26	PB3
PA4/T0CKI	8	25	PB2
PA5/AIC4	9	24	PB1
VSS	10	23	PB0/INT
PA6/AIC5	11	22	VDD
PA7/AIC6	12	21	VSS
PC0/T1OSO/T1CKI	13	20	PC7
PC1/T1OSI	14	19	PC6
PC2/CCP	15	18	PC5
PC3	16	17	PC4

MDT14F201P11 (PDIP)

/MCLR	1	28	PB7
PA0/AIC0	2	27	PB6
PA1/AIC1	3	26	PB5
PA2/AIC2	4	25	PB4
PA3/AIC3/Vref	5	24	PB3
PA4/T0CKI	6	23	PB2
PA5/AIC4	7	22	PB1
VSS	8	21	PB0/INT
PA6/AIC5	9	20	VDD
PA7/AIC6	10	19	VSS
PC0/T1OSO/T1CKI	11	18	PC7
PC1/T1OSI	12	17	PC6
PC2/CCP	13	16	PC5
PC3	14	15	PC4

MDT14F201K11 (SKINNY)

MDT14F201S11 (SOP)



MDT14F201LQ11 (LQFP)

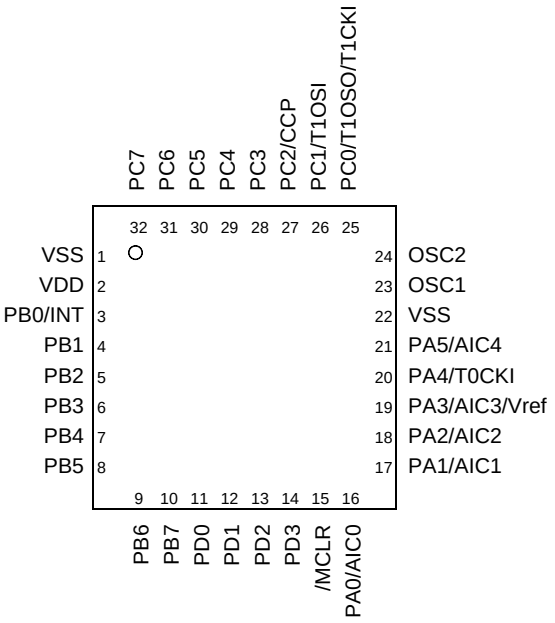
PD2	1	32	PD1
PD3	2	31	PD0
/MCLR	3	30	PB7
PA0/AIC0	4	29	PB6
PA1/AIC1	5	28	PB5
PA2/AIC2	6	27	PB4
PA3/AIC3/Vref	7	26	PB3
PA4/T0CKI	8	25	PB2
PA5/AIC4	9	24	PB1
VSS	10	23	PB0/INT
OSC1	11	22	VDD
OSC2	12	21	VSS
PC0/T1OSO/T1CKI	13	20	PC7
PC1/T1OSI	14	19	PC6
PC2/CCP	15	18	PC5
PC3	16	17	PC4

MDT14F201P12 (PDIP)

/MCLR	1	28	PB7
PA0/AIC0	2	27	PB6
PA1/AIC1	3	26	PB5
PA2/AIC2	4	25	PB4
PA3/AIC3/Vref	5	24	PB3
PA4/T0CKI	6	23	PB2
PA5/AIC4	7	22	PB1
VSS	8	21	PB0/INT
OSC1	9	20	VDD
OSC2	10	19	VSS
PC0/T1OSO/T1CKI	11	18	PC7
PC1/T1OSI	12	17	PC6
PC2/CCP	13	16	PC5
PC3	14	15	PC4

MDT14F201K12 (SKINNY)

MDT14F201S12 (SOP)



MDT14F201LQ12 (LQFP)

5. Pin Function Description

Pin Name	I/O	Function Description
PA0~PA3, PA5	I/O	Port A, TTL input level / Analog input channel
PA4	I/O	PA4, Schmitt Trigger input levels, Open drain output
PB0~PB7	I/O	Port B, TTL input level / PB0: External interrupt input PB4~PB7: Interrupt on pin change
PC0~PC7	I/O	Port C, Schmitt Trigger input levels
PD0~3	I/O	Port D, Schmitt Trigger input levels
/MCLR	I	Master Clear, Schmitt Trigger input levels
OSC1/CLKIN/PA6	I, I/O	Oscillator Input / external clock input. PA6/ Analog input channel in IRC mode.
OSC2/CLKOUT/PA7	O, I/O	Oscillator Output / in RC mode, the CLKOUT pin has 1/4 frequency of CLKIN. PA7/ Analog input channel in IRC mode.
VDD		Power supply
VSS		Ground

6. Memory Map

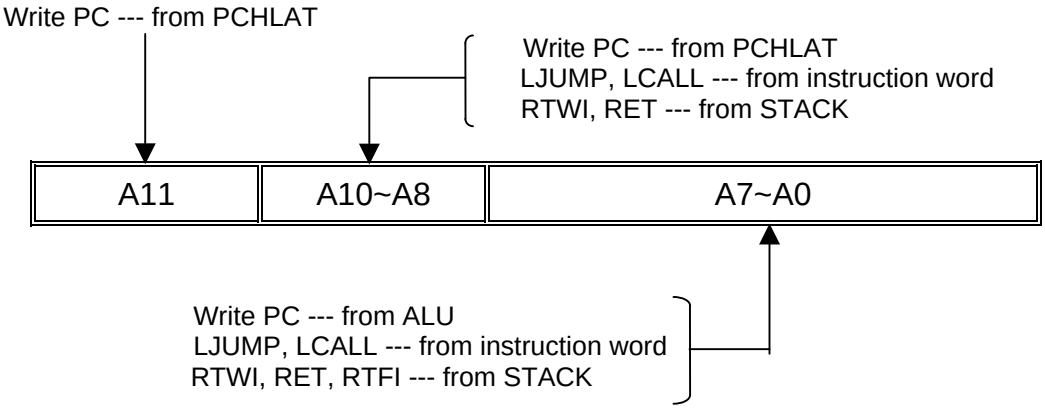
(A) Register Map

Address	Description	Address	Description
BANK0		**BANK1**	
00	IAR	80	IAR
01	RTCC	81	TMR
02	PCL	82	PCL
03	STATUS	83	STATUS
04	MSR	84	MSR
05	Port A	85	CPIO A
06	Port B	86	CPIO B
07	Port C	87	CPIO C
08	Port D	88	CPIO D
09	TTLCTL0	89	TTLCTL1
0A	PCHLAT	8A	-
0B	INTS	8B	-
0C	PIFB1	8C	PIEB1
0D	-	8D	-
0E	TMR1L	8E	PSTA
0F	TMR1H	8F	PAPHR
10	T1STA	90	PBPHR
11	TMR2	91	-
12	T2STA	92	T2PER
13	DBCTL	93	-
14		94	-
15	CCP1L	95	PCPHR
16	CCP1H	96	PDPHR
17	CCP1CTL	97	-
18	-	98	-
19	-	99	-
1A	-	9A	EEDATA
1B	-	9B	EEADR
1C	-	9C	EECON1
1D	-	9D	EECON2
1E	ADRES	9E	ADRES
1F	ADS0	9F	ADS1
20~7F	General purpose register	A0~FF	General purpose register

(1) IAR (Indirect Address Register): R00

(2) RTCC (Real Time Counter/Counter Register): R01

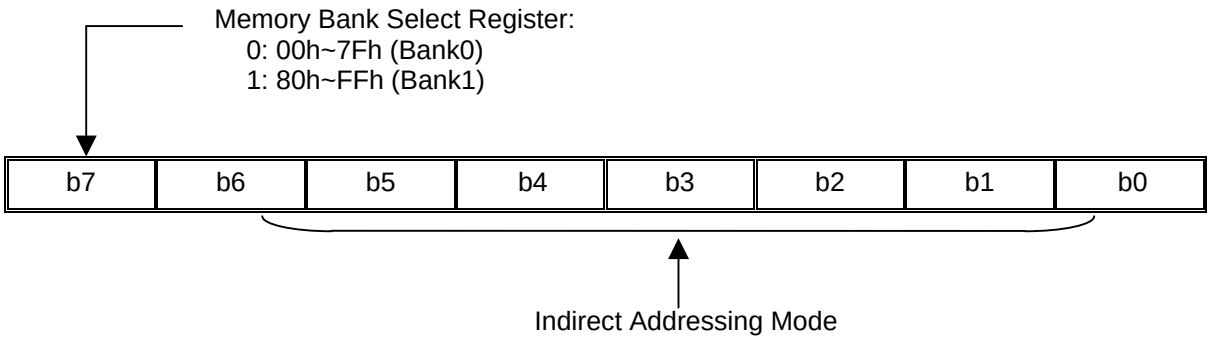
(3) PC (Program Counter): R02, R0A



(4) STATUS (Status register): R03

Bit	Symbol	Function
0	C	Carry bit
1	HC	Half Carry bit
2	Z	Zero bit
3	/PF	Power down bit
4	/TF	WDT timer overflow bit
5	RBS0	Register Bank select bit 0: 00h~7Fh (Bank0) 1: 80h~FFh (Bank1)
7~6	--	General purpose bit

(5) MSR (Memory Bank Select Register): R04



(6) PORT A: R05
PA5~PA0, I/O Register

(7) PORT B: R06
PB7~PB0, I/O Register

(8) PORT C: R07
PC7~PC0, I/O Register

(9) PORT D:R08
PD3~PD0, I/O Register

(10) TTLCTL0: R09

Bit	Symbol	Function
0	PB1OUT	PB1OUT in TTL MODE circuit
1	PC2OUT	PC2OUT in TTL MODE circuit
2	EABS	EABS function enable
3	LSOUTS	Low side output active selection
4	HSOUTS	High side output active selection
7~5	PRSCLL2~0	Low side Delay time set 000 : 0 clock 001 : 1 clock : 111 : 7 clocks

(11) PCHLAT: R0A

(12) INTS (Interrupt Status Register): R0B

Bit	Symbol	Function
0	RBIF	PORT B change interrupt flag, Set when PB <7:4> inputs change
1	INTF	Set when INT interrupt occurs
2	TIF	Set when TMR0 overflows
3	RBIE	0: Disable PB change interrupt 1: Enable PB change interrupt
4	INTS	0: Disable INT interrupt 1: Enable INT interrupt
5	TIS	0: Disable TMR0 interrupt 1: Enable TMR0 interrupt
6	PEIE	0: Disable all peripheral interrupt 1: Enable all peripheral interrupt
7	GIS	0: Disable global interrupt 1: Enable global interrupt

(13) PIFB1 (Peripheral Interrupt Flag Bit): R0C

Bit	Symbol	Function
0	TMR1IF	TMR1 interrupt flag 0: TMR1 did not overflow 1: TMR1 overflowed
1	TMR2IF	TMR2 interrupt flag 0: No TMR2 to T2PER match occurred 1: TMR2 to T2PER match occurred
2	CCP1IF	CCP1 interrupt flag 0: No TMR1 capture/compare occurred 1: A TMR1 capture/compare occurred
5~3	--	Unimplemented
6	ADIF	A/D interrupt flag 0: A/D conversion is not complete 1: A/D conversion completed
7	--	Unimplemented

(14) TMR1L: R0E

The LSB of the 16-bit TMR1

(15) TMR1H: R0F

The MSB of the 16-bit TMR1

(16) T1STA: R10

Bit	Symbol	Function
0	TMR1ON	0: Stop TMR1 1: Enable TMR1
1	TMR1CLK	0: Internal clock (Fosc/4) 1: External clock from pin PC0
2	/T1SYNC	TMR1CLK = 1 0: Synchronize external clock 1: Do not synchronize external clock TMR1CLK = 0 This bit is ignored
3	T1OSCEN	0: TMR1 Oscillator is shut off 1: TMR1 Oscillator is enable

Bit	Symbol	Function
5~4	T1CKPS1 ~ T1CKPS0	1 1 = 1:8 Prescale value 1 0 = 1:4 Prescale value 0 1 = 1:2 Prescale value 0 0 = 1:1 Prescale value
7~6	--	Unimplemented

(17) TMR2: R11

TMR2 register

(18) T2STA: R12

Bit	Symbol	Function
1~0	T2CKPS1 ~ T2CKPS0	0 0 = Prescaler is 1 0 1 = Prescaler is 4 1 x = Prescaler is 16
2	TMR2ON	0: TMR2 is off 1: TMR2 is on
7~3	--	Unimplemented

(19) DBCTL: R13

PB0 input de-bounce control register

Bit	Symbol	Function
0	DBEN	0: Disable PB0 input de-bounce 1: Enable PB0 input de-bounce
4~1	DEBNL3 ~ DEBNL0	Low pulse de-bounce control If Fosc=16MHz, detect pulse 0000:0uS, 0001:1uS, 0010:2uS, ~ ,1111:15uS
7~5	DEBNH2 ~ DEBNH0	How pulse de-bounce control If Fosc=16MHz, detect pulse 000:0uS, 001:1uS, 010:2uS, ~ ,111:7uS

(20) CCP1L: R15

Capture/Compare/PWM LSB

(21) CCP1H: R16

Capture/Compare/PWM MSB

(22) CCP1CTL: R17

Bit	Symbol	Function
3~0	CCP1M3 ~ CCP1M0	0 0 0 0: CCP1 off 0 1 0 0: Capture1 mode, every falling edge 0 1 0 1: Capture1 mode, every rising edge 0 1 1 0: Capture1 mode, every 4th rising edge 0 1 1 1: Capture1 mode, every 16th rising edge 1 0 0 0: Compare1 mode, set output on match 1 0 0 1: Compare1 mode, clear output on match 1 0 1 0: Compare1 mode, generate software interrupt on match 1 0 1 1: Compare1 mode, trigger special event 1 1 x x: PWM1 mode
5~4	PWM1LSB	These bits are the two LSBs of the PWM1 duty cycle
7~6	--	Unimplemented

(23) ADRES: R1E

A/D result register

(24) ADS0 (A/D Status Register): R1F

Bit	Symbol	Function
0	ADRUN	0: A/D converter module is shut off and consumes no operating current 1: A/D converter module is operating
1	--	Unimplemented
2	GO/DONEB	0: A/D conversion not in progress 1: A/D conversion in progress
5~3	CHS2~0	000: AIC0 001: AIC1 010: AIC2 011: AIC3 100: AIC4 101: AIC5 110: AIC6
7~6	ASCS1-0	00: fosc/2 01: fosc/8 10: fosc/32 (*Note1) 11: f RC (*Note2)

*Note1: for HF or IRC

*Note2: determined by OSC mode, HF: fosc/32, XT: fosc/8, RC: fosc/2, LF: fosc/2

(25) TMR (Time Mode Register): R81

Bit	Symbol	Function		
2~0	PS2~0	Prescaler Value	RTCC rate	WDT rate
		0 0 0	1 : 2	1 : 1
		0 0 1	1 : 4	1 : 2
		0 1 0	1 : 8	1 : 4
		0 1 1	1 : 16	1 : 8
		1 0 0	1 : 32	1 : 16
		1 0 1	1 : 64	1 : 32
		1 1 0	1 : 128	1 : 64
		1 1 1	1 : 256	1 : 128
3	PSC	Prescaler assignment bit 0: RTCC 1: Watchdog Timer		
4	TCE	RTCC signal edge 0: Increment on low-to-high transition on RTCC pin 1: Increment on high-to-low transition on RTCC pin		
5	TCS	RTCC signal set 0: Internal instruction cycle clock 1: Transition on RTCC pin		
6	IES	Interrupt edge select 0: Interrupt on falling edge on PB0 1: Interrupt on rising edge on PB0		
7	PBPH	PORTB7~0 pull-hi 0: PORTB7~0 pull-hi are enable 1: PORTB7~0 pull-hi are disable		

(26) CPIO A (Control Port I/O Mode Register): R85
＝“0”, I/O pin in output mode;
＝“1”, I/O pin in input mode.

(27) CPIO B (Control Port I/O Mode Register): R86
＝“0”, I/O pin in output mode;
＝“1”, I/O pin in input mode.

(28) CPIO C (Control Port I/O Mode Register): R87
＝“0”, I/O pin in output mode;
＝“1”, I/O pin in input mode.

(29) CPIO D (Control Port I/O Mode Register): R88
＝“0”, I/O pin in output mode;
＝“1”, I/O pin in input mode.

(30) TTLCTL1: R89

Bit	Symbol	Function
0	TTLMOD	0: Disable TTL MODE 1: Enable TTL MODE
1	OVLEN	Over load protect enable
3~2	PRDIV1~0	Clock input division 00=Fosc/2; 01=Fosc/4; 10=Fosc/8; 11=Fosc/16
7~4	PRSCL3~0	Delay time set 0000 : 0 clock 0001 : 1 clock 0010 : 2 clocks : 1111 : 15 clocks

(31) PIEB1: R8C

Bit	Symbol	Function
0	TMR1IE	TMR1 interrupt enable bit 0: Disable TMR1 interrupt 1: Enable TMR1 interrupt
1	TMR2IE	TMR2 interrupt enable bit 0: Disable TMR2 interrupt 1: Enable TMR2 interrupt
2	CCP1IE	CCP1 interrupt enable bit 0: Disable CCP1 interrupt 1: Enable CCP1 interrupt
5~3	--	Unimplemented
6	ADIE	A/D interrupt enable bit 0: Disable A/D interrupt 1: Enable A/D interrupt
7	--	Unimplemented

(32) PSTA: R8E

Bit	Symbol	Function
0	PEDHB	0: Power-edge detector high level reset occurred 1: No Power-edge detector high level reset occurred
1	PORB	0: Power on Reset occurred 1: No Power on Reset occurred
7~2	--	Unimplemented

(33) PAPHR: R8F

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PAPHR	PHA7	PHA6	PHA5	-	PHA3	PHA2	PHA1	PHA0

Port A Pull_hi Control Bits
0 = Pull_hi disable
1 = Pull_hi enable

(34) PBPHR: R90

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PBPHR	PHB7	PHB6	PHB5	PHB4	PHB3	PHB2	PHB1	PHB0

Port B Pull_hi Control Bits
0 = Pull_hi disable
1 = Pull_hi enable

(35) T2PER: R92
Timer2 period

(36) PCPHR: R95

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCPHR	PHC7	PHC6	PHC5	PHC4	PHC3	PHC2	PHC1	PHC0

Port C Pull_hi Control Bits
0 = Pull_hi disable
1 = Pull_hi enable

(37) PDPHR: R96

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PDPHR	-	-	-	-	PHD3	PHD2	PHD1	PHD0

Port D Pull_hi Control Bits
0 = Pull_hi disable
1 = Pull_hi enable

(38) EEDATA(EEPROM data register.):R9A

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EEDATA	EED7	EED6	EED5	EED4	EED3	EED2	EED1	EED0

(39) EEADR (EEPROM address register):R9B.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EEADR	-	EEAD6	EEAD5	EEAD4	EEAD3	EEAD2	EEAD1	EEAD0

(40) EECON (EEPROM control register 1):R9C.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EECON1	-	-	-	-	WRERR	WREN	WR	RD

WRERR : EEPROM Write Error Flag Bit.
0 = The EEPROM write operation completed
1 = The EEPROM write operation is prematurely terminated

(any MCLR reset or any WDT reset during normal operation)

WREN : EEPROM Write Enable Bit.

0 = Inhibits write to the data EEPROM

1 = Allows write cycles

WR : Write Control Bit.

0 = Write cycle to the data EEPROM is complete

1 = Initiates a write cycle. (The bit is cleared by hardware once write is complete. The WR bit can only be set (not clear) in software.)

RD : Read Control Bit.

0 = Does not initiate an EEPROM read.

1 = Initiates an EEPROM read (read takes once cycle. RD is cleared in hardware. The RD bit can only be set (not clear) in software.)

(41) EECON2(EEPROM control register 2): R9D.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EECON2	-	-	-	-	-	-	-	-

Write only ; Read as “0”

When write data to the EEPROM must write 55/H to EECCON2, and writ AA/H to EECCON2 then set WR bit; the EEPROM can write data inside for write each byte.

Example : Data EEPROM Write

```
BSR     STATUS, PAGE    ; Select bank1
BCR     INTS, GIS       ; Disable interrupt
BSR     EECON1, WREN    ; Enable write
LDWI    55H
STWR    EECON2          ; Write 55/H
LDWI    0AAH
STWR    EECON2          ; Write AA/H
BSR     EECON1, WR      ; Begin write
```

(42) ADS1 (A/D Status Register): R9F

Bit	Symbol	Function
2~0	PAVM2~0	0 0 0: PA0~3,PA5 = analog input, PA6~7 = analog input, VREF = VDD 0 0 1: PA0~2,PA5 = analog input, PA6~7 = analog input, VREF = PA3 0 1 0: PA0~3,PA5 = analog input, PA6~7 = digital input, VREF = VDD 0 1 1: PA0~2,PA5 = analog input, PA6~7 = digital input, VREF = PA3 1 0 0: PA0, 1, 3 = analog input, PA2, 5 = digital I/O, PA6~7 = digital input, VREF = VDD 1 0 1: PA0, 1 = analog input, PA2, 5 = digital I/O, PA6~7 = digital input, VREF = PA3 1 1 x PA0~3, 5 = digital I/O
7~3	--	Unimplemented

Configurable options for FLASH ROM (Set by writer)

Oscillator Type	
MDT14F201 P12/S12/K12/LQ12	MDT14F201 P11/S11/K11/LQ11
RC Oscillator	IRC 16M Oscillator
HFXT Oscillator	
XTAL Oscillator	
LFXT Oscillator	

Watchdog Timer control
Watchdog timer disable all the time
Watchdog timer enable all the time

Power-edge Detect
Power-edge Detect disable
Low level around 1.8V
Middle level around 2.1V
High level around 3.8V

Oscillator-start Timer control
0ms
75ms

Security state
Security Disable
Security Enable

(B) Program Memory

Address	**Description**
000-FFF	Program memory
000	The starting address of power on, external reset or WDT time-out reset.
004	Interrupt vector

7. Reset Condition for all Registers

Register	Address	Power-On Reset, Power edge detector high level Reset	/MCLR or WDT Reset	Wake-up from SLEEP
IAR	00h	N/A	N/A	N/A
RTCC	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PC	0Ah,02h	0000 0000 0000	0000 0000 0000	PC+1
STATUS	03h	0001 1xxx	000# #uuu	000# #uuu
MSR	04h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORT A	05h	--xx xxxx	--uu uuuu	--uu uuuu
PORT B	06h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORT C	07h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORT D	08h	---- xxxx	---- uuuu	---- uuuu
TTLCTL0	09h	0000 0000	0000 0000	uuuu uuuu
PCHLAT	0Ah	---0 0000	---0 0000	---u uuuu
INTS	0Bh	0000 000x	0000 000u	uuuu uuuu
PIFB1	0Ch	-0-- -000	-0-- -000	-u-- -uuu
TMR1L	0Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1H	0Fh	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1STA	10h	--00 0000	--uu uuuu	--uu uuuu
TMR2	11h	0000 0000	0000 0000	uuuu uuuu
T2STA	12h	---- -000	---- -uuu	---- -uuu
DBCTL	13h	0000 0000	0000 0000	uuuu uuuu
CCP1L	15h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP1H	16h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP1CTL	17h	--00 0000	--00 0000	--uu uuuu
ADRES	1Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADS0	1Fh	0000 00-0	0000 00-0	uuuu uu-u
TMR	81h	1111 1111	1111 1111	uuuu uuuu
CPIOA	85h	--11 1111	--11 1111	--uu uuuu
CPIOB	86h	1111 1111	1111 1111	uuuu uuuu
CPIOC	87h	1111 1111	1111 1111	uuuu uuuu
CPIOD	88h	---- 1111	---- 1111	---- uuuu

Register	Address	Power-On Reset, Power range detector Reset	/MCLR or WDT Reset	Wake-up from SLEEP
TTLCTL1	89h	0000 0000	0000 0000	uuuu uuuu
PIEB1	8Ch	-0-- -000	-0-- -000	-u-- -uuu
PSTA	8Eh	---- --0u	---- --uu	---- --uu
T2PER	92h	1111 1111	1111 1111	1111 1111
ADS1	9Fh	---- -000	---- -000	---- -uuu

Note : u=unchanged, x=unknown, - =unimplemented, read as "0"

#=value depends on the condition of the following table

Condition	Status: bit 4	Status: bit 3	PSTA: bit 1	PSTA: bit 0
/MCLR reset (not during SLEEP)	u	u	u	u
/MCLR reset during SLEEP	1	0	u	u
WDT reset (not during SLEEP)	0	1	u	u
WDT reset during SLEEP	0	0	u	u
Power-on reset	1	1	0	x
Power-edge high level reset	1	1	u	0

Note : u=unchanged, x=unknown, - =unimplemented, read as "0"

8. Instruction Set

Instruction Code	Mnemonic Operands	Function	Operating	Status
010000 00000000	NOP	No operation	None	
010000 00000001	CLRWT	Clear Watchdog timer	0→WT	TF, PF
010000 00000010	SLEEP	Sleep mode	0→WT, stop OSC	TF, PF
010000 00000011	TMODE	Load W to TMODE register	W→TMODE	None
010000 00000100	RET	Return from subroutine	Stack→PC	None
010000 00000rrr	CPIO R	Control I/O port register	W→CPIO R	None
010001 1rrrrrrr	STWR R	Store W to register	W→R	None
011000 trrrrrrr	LDR R, t	Load register	R→t	Z
111010 iiiiiiii	LDWI i	Load immediate to W	i→W	None
010111 trrrrrrr	SWAPR R, t	Swap halves register	[R(0~3) ↔R(4~7)] →t	None
011001 trrrrrrr	INCR R, t	Increment register	R + 1→t	Z
011010 trrrrrrr	INCRSZ R, t	Increment register, skip if zero	R + 1→t	None
011011 trrrrrrr	ADDWR R, t	Add W and register	W + R→t	C, HC, Z

Instruction Code	Mnemonic Operands	Function	Operating	Status
011100 trrrrrrr	SUBWR R, t	Subtract W from register	R – W→t or (R+/W+1→t)	C, HC, Z
011101 trrrrrrr	DECR R, t	Decrement register	R – 1→t	Z
011110 trrrrrrr	DECRSZ R, t	Decrement register, skip if zero	R – 1→t	None
010010 trrrrrrr	ANDWR R, t	AND W and register	R ∩ W→t	Z
110100 iiiiiiii	ANDWI i	AND W and immediate	i ∩ W→W	Z
010011 trrrrrrr	IORWR R, t	Inclu. OR W and register	R ∪ W→t	Z
110101 iiiiiiii	IORWI i	Inclu. OR W and immediate	i ∪ W→W	Z
010100 trrrrrrr	XORWR R, t	Exclu. OR W and register	R ⊕ W→t	Z
110110 iiiiiiii	XORWI i	Exclu. OR W and immediate	i ⊕ W→W	Z
011111 trrrrrrr	COMR R, t	Complement register	/R→t	Z
010110 trrrrrrr	RRR R, t	Rotate right register	R(n) →R(n-1), C→R(7), R(0)→C	C
010101 trrrrrrr	RLR R, t	Rotate left register	R(n)→r(n+1), C→R(0), R(7)→C	C
010000 1xxxxxxx	CLRW	Clear working register	0→W	Z
010001 0rrrrrrr	CLRR R	Clear register	0→R	Z
0000bb brrrrrrr	BCR R, b	Bit clear	0→R(b)	None
0010bb brrrrrrr	BSR R, b	Bit set	1→R(b)	None
0001bb brrrrrrr	BTSC R, b	Bit Test, skip if clear	Skip if R(b)=0	None
0011bb brrrrrrr	BTSS R, b	Bit Test, skip if set	Skip if R(b)=1	None
100nnn nnnnnnnn	LCALL n	Long CALL subroutine	n→PC, PC+1→Stack	None
101nnn nnnnnnnn	LJUMP n	Long JUMP to address	n→PC	None
110111 iiiiiiii	ADDWI i	Add immediate to W	W+i→W	C,HC,Z
110001 iiiiiiii	RTWI i	Return, place immediate to W	Stack→PC,i→W	None
111000 iiiiiiii	SUBWI i	Subtract W from immediate	i-W→W	C,HC,Z
010000 00001001	RTFI	Return from interrupt	Stack→PC,1→GIS	None

Note :

W	:	Working register	b	:	Bit position
WT	:	Watchdog timer	t	:	Target
TMODE	:	TMODE mode register		0	: Working register
CPIO	:	Control I/O port register		1	: General register
TF	:	Timer overflow flag	R	:	General register address
PF	:	Power loss flag	C	:	Carry flag
PC	:	Program Counter	HC	:	Half carry
OSC	:	Oscillator	Z	:	Zero flag
Inclu.	:	Inclusive '∪'	/	:	Complement
Exclu.	:	Exclusive '⊕'	x	:	Don't care
AND	:	Logic AND '∩'	i	:	Immediate data (8 bits)
			n	:	Immediate address

9.Electrical Characteristics

*Note: Temperature=25°C

(a)・Operation Current::

WORK	OSC TYPE:IRC PUT:75ms WDT:disable PED:Disable
	IC1 16MHz
6.4V	6.04m
6.0V	5.47m
5.0V	4.14m
4.0V	2.99m
3.0V	2.04m
2.5V	1.63m

SLEEP	OSC TYPE:IRC PUT:75ms WDT:Enable PED:Disable
	IC1 16MHz
6.4V	11.8u
6.0V	10.2u
5.0V	6.4u
4.0V	3.6u
3.0V	1.6u
2.5V	1.0u

WORK	OSC TYPE:HF PUT:75ms WDT:Disable PED:Disable		
IC1	4M C:20	10M C:20P	20M C:20P
5.0V	1.53m	3.03m	5.11m
4.0V	1.02m	2.16m	3.73m
3.0V	642u	1.42m	2.51m
2.5V	483u	1.10m	1.98m
2.3V	427u	990u	1.77m

WORK		OSC TYPE:LF PUT:75ms WDT:Disable PED:Disable	
VDD=5V		IC1	
20p	4.7K	5.26M	2.15m
	10K	2.68M	1.20m
	47K	604.84K	440u
	100K	289.86K	325u
	300K	97.40K	254u
	470K	61.98K	240u
100p	4.7K	1.72M	1.34m
	10K	857.14K	770u
	47K	189.87K	338u
	100K	90.36K	275u
	300K	30.30K	235u
	470K	19.11K	226u

WORK		OSC TYPE:LF PUT:75ms WDT:Disable PED:Disable	
VDD=5V		IC1	
300p	4.7K	691.24K	1.09m
	10K	340.91K	639u
	47K	75.00K	310u
	100K	35.50K	262u
	300K	11.90K	229u
	470K	7.58K	222u

(b)、Output Voltage (VDD = 5V /3V):

(@VDD=5V)	PA		PA4 (open drain)	PB		PC		PD	
Output	HIGH	LOW	LOW	HIGH	LOW	HIGH	LOW	HIGH	LOW
condition=5mA	4.58V	117.5 mV	195.8 mV	4.56V	119.4 mV	4.57V	117.9 mV	4.58V	119.2mV
condition=20mA	3.48V	488 mV	813 mV	3.44V	497 mV	3.41V	489 mV	3.54V	497 mV
Input	36.2mA	61.2 mA	42.2 mA	36.1 mA	60.8 mA	35.9 mA	59.5 mA	36.1 mA	60.5 mA

(@VDD=3V)	PA		PA4 (open drain)	PB		PC		PD	
Output	HIGH	LOW	LOW	HIGH	LOW	HIGH	LOW	HIGH	LOW
condition=5mA	2.45V	148 mV	322 mV	2.44V	151 mV	2.24V	150 mV	2.44V	151 mV
condition=10mA	1.83V	310 mV	726 mV	1.8V	316 mV	1.8V	316 mV	1.8V	317 mV
Input	14.32 mA	30.4 mA	17.3 mA	14.18 mA	30.1 mA	14.24 mA	29.2 mA	14.15 mA	30 mA

Max output driver

VDD	5V	3V
Max driver	PA output pin*5	PA output pin*5
Sourse current h	166.5mA	105.6mA
Sink current l	250mA	154.4mA
Max driver	PB output pin*8	PB output pin*8
Sourse current h	250mA	107.1mA
Sink current l	250mA	200mA
Max driver	PC output pin*8	PC output pin*8
Sourse current h	250mA	150.4mA
Sink current l	250mA	210mA
Max driver	PD output pin*4	PD output pin*4
Sourse current h	136.8mA	55.2mA
Sink current l	220mA	111.3mA

(c)、Input Voltage (VDD = 5V/3V):

(@VDD=5V)	PA0~3,5	PA4	PB	PC	PD
	TTL	ST	TTL	ST	ST
HIGH	1.658V	3.4V	1. 60V	2.84V	2.96V
LOW	1.454V	2.08V	1.52V	1.28V	1.28V
(@VDD=3V)	PA0~3,5	PA4	PB	PC	PC
	TTL	ST	TTL	ST	ST
HIGH	1.20V	2.0V	1.20V	1.64V	1.76V
LOW	1.12V	1.52V	1.12V	1.00V	1.00V

(d)、Pull high/low resistor：

	IC1
Pull high	PB
5V	49.6
3V	92.59

(e)、he basic WDT time-out cycle time

@Temperature＝25 ℃, the typical value as followings :

V_{dd} =5.0 V, Temperature=25℃,the typical value as followings

	2.0V	2.5V	3.0V	4.0V	5.0V
1:1	29.2 ms	26.4 ms	24.4 ms	21.4 ms	19.6 ms
1:2	58.4 ms	52.8 ms	48.8 ms	43.2 ms	39.6 ms
1:4	117 ms	106 ms	97 ms	87 ms	79 ms
1:8	233 ms	211 ms	195 ms	173 ms	158 ms
1:16	464 ms	416 ms	384 ms	344 ms	312 ms
1:32	936 ms	848 ms	784 ms	688 ms	632 ms
1:64	1.88 s	1.68 s	1.56 s	1.38 s	1.26 s
1:128	3.76 s	3.32 s	3.16 s	2.76 s	2.52 s

(f)、Power Edge-detector Reset Voltage (Not in Sleep Mode), @ V_{dd}＝5.0 V (PED : Enable)

	Low	Middle	High
HI TO LOW	1.73V	2.21V	3.65V
LOW TO HI	1.75V	2.26V	4.12V