1. General Description

This EPROM-Based 8-bit micro-controller uses a fully static CMOS technology process to achieve higher speed and smaller size with the low power consump-tion and high noise immunity. On chip memory includes 1K words of ROM, and 64 bytes of static RAM.

2. Features

The followings are some of the features on the hardware and software :

- Fully CMOS static design
- 8-bit data bus
- On chip ROM size : 1K words
- Internal RAM size : 64 bytes
- 37 single word instructions
- 14-bit instructions
- 8-level stacks
- Operating voltage : 2.5 V ~ 5.5 V
- Built in 8MHz, 4MHz internal RC
- Oscillator can be selected by programming option:

  INTRC－Internal 8MHz/4MHz
- Addressing modes include direct, indirect and relative

  addressing modes
- Power-on Reset
- Power edge-detector Reset
- Sleep Mode for power saving
- 8-bit real time clock/counter(RTCC) with 8-bit programmable prescaler
- Soft-ware I/O pull-up/down or open-drain control
- On-chip RC oscillator based Watchdog Timer(WDT)
- Timer 1: 8-bit PWM/counter with 8 bit period
- five interrupt source：

  -External INT Pin (PB0)

  -Timer0

  -PB5~1 Interrupt on pin change

  -PA5~0 Interrupt on pin change

  -TMR1 and PR1 Compare

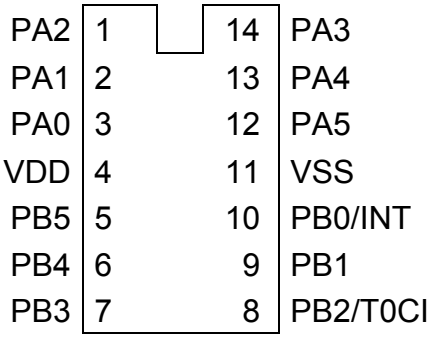
	PINS	I/O	OSC
MDT10P611P12	14	12	IRC 8MHz/4MHz
MDT10P611S12	14	12	

3. Applications

The application areas of this 10P611 range from appliance motor control and high speed automotive to low power remote transmitters/receivers, small instruments, toy, automobile.

4. Pin Assignment

10P611P12/S12



5. Pin Function Description

Pin Name	I/O	Function Description
PA5~0	I/O	Port A, TTL input level. PA5~PA0: Interrupt on pin change. Software select PWM2 output Software controlled pull-high (100K/5V) /pull-low (100K/5V) /open-drain.
PB5~0	I/O	Port B, TTL input level PB0: External INT input. PB5~PB1: Interrupt on pin change. PB5、4、2、1 Software select PWM1 output Software controlled pull-high (100K/5V) /pull-low (100K/5V) /open-drain. PB3 input only.
VDD		Power supply
VSS		Ground

6. Memory Map

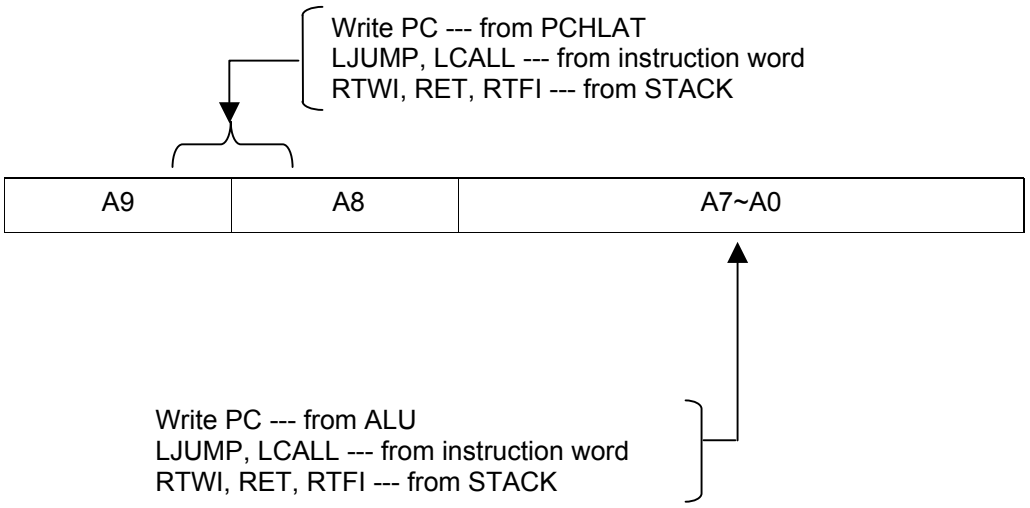
(A) Register Map

Address	Description
Bank 0	
00	Indirect Addressing Register
01	RTCC
02	PCL
03	STATUS
04	MSR
05	Port A
06	Port B
08	PBIE
09	PBIF
0A	PCHLAT
0B	INTS
0C	/PHPB
0D	/PLPB
0E	/ODPB
10~4F	64 bytes General purpose registers
50	TMR1
51	PR1
52	Duty cycle1
53	T1CON
54	Duty cycle2
55	CHSA
Bank 1	
01	TMR0
05	CPIO A
06	CPIO B
07	PSTA
08	PAIE
09	PAIF
0C	/PHPA
0D	/PLPA
0E	/ODPA

(1) IAR (Indirect Address Register): R0

(2) RTCC (Real Time Clock/Counter register): R01

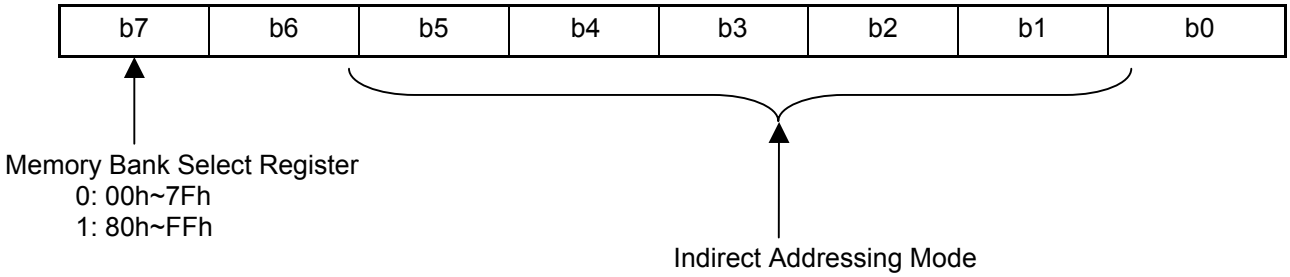
(3) PC (Program Counter): R02, R0A



(4) STATUS (Status register): R3

Bit	Symbol	Function
0	C	Carry bit
1	HC	Half Carry bit
2	Z	Zero bit
3	PF	Power down bit
4	TF	WDT Timer overflow Flag bit
5	RBS0	Register Bank select bit 0: 00h~7Fh 1: 80h~FFh
7~6	--	General Purpose bit

(5) MSR (Memory Bank Select Register): R4



(6) PORT A: R05
PA5~PA0, I/O register.

(7) PORT B: R06
PB5~PB0, I/O register, PB3 input only.

(8) PBIE: R08

Bit	Symbol	Function
0	--	Reserved, Read as “0”
1	PB1IE	0: Disable PB1 pin change interrupt 1: Enable PB1 pin change interrupt
2	PB2IE	0: Disable PB2 pin change interrupt 1: Enable PB2 pin change interrupt
3	PB3IE	0: Disable PB3 pin change interrupt 1: Enable PB3 pin change interrupt
4	PB4IE	0: Disable PB4 pin change interrupt 1: Enable PB4 pin change interrupt
5	PB5IE	0: Disable PB5 pin change interrupt 1: Enable PB5 pin change interrupt
7~6	--	Reserved, Read as “0”

(9) PBIF: R09

Bit	Symbol	Function
0	--	Reserved, Read as “0”
1	PB1IF	0: No PB1 pin change interrupt occurred 1: The PB1 pin change interrupt occurred
2	PB2IF	0: No PB2 pin change interrupt occurred 1: The PB2 pin change interrupt occurred
3	PB3IF	0: No PB3 pin change interrupt occurred 1: The PB3 pin change interrupt occurred
4	PB4IF	0: No PB4 pin change interrupt occurred 1: The PB4 pin change interrupt occurred
5	PB5IF	0: No PB5 pin change interrupt occurred 1: The PB5 pin change interrupt occurred
7~6	--	Reserved, Read as “0”

(10) INTS: R0B

Bit	Symbol	Function
0	--	Reserved, Read as “0”
1	INTF	Set when INT interrupt occurs INT interrupt flag.
2	TIF	Set when TMR0 overflows.
3	--	Reserved, Read as “0”
4	INTS	0: Disable INT interrupt 1: Enable INT interrupt
5	TIS	0: Disable TMR0 interrupt 1: Enable TMR0 interrupt

Bit	Symbol	Function
6	TMR1E	Timer1 and PR1 Compare 0:TMR1 interrupt disable 1:TMR1 interrupt enable
7	GIS	0: Disable global interrupt 1: Enable global interrupt

(11) /PHPB: R0C

Bit	Symbol	Function
0	/PHPB0	0: Enable PB0 internal pull-high 1: Disable PB0 internal pull-high
1	/PHPB1	0: Enable PB1 internal pull-high 1: Disable PB1 internal pull-high
2	/PHPB2	0: Enable PB2 internal pull-high 1: Disable PB2 internal pull-high
3	--	Reserved, Read as “0”
4	/PHPB4	0: Enable PB4 internal pull-high 1: Disable PB4 internal pull-high
5	/PHPB5	0: Enable PB5 internal pull-high 1: Disable PB5 internal pull-high
7~6	--	Reserved, Read as “0”

(12) /PLPB: R0D

Bit	Symbol	Function
0	/PLPB0	0: Enable PB0 internal pull-low 1: Disable PB0 internal pull-low
1	/PLPB1	0: Enable PB1 internal pull-low 1: Disable PB1 internal pull-low
2	/PLPB2	0: Enable PB2 internal pull-low 1: Disable PB2 internal pull-low
3	--	Reserved, Read as “0”
4	/PLPB4	0: Enable PB4 internal pull-low 1: Disable PB4 internal pull-low
5	/PLPB5	0: Enable PB5 internal pull-low 1: Disable PB5 internal pull-low
7~6	--	Reserved, Read as “0”

(13) ODPB: R0E

Bit	Symbol	Function
0	ODPB0	0: Disable PB0 open-drain 1: Enable PB0 open-drain
1	ODPB1	0: Disable PB1 open-drain

Bit	Symbol	Function
		1: Enable PB1 open-drain
2	ODPB2	0: Disable PB2 open-drain 1: Enable PB2 open-drain
3	--	Reserved, Read as “0”
4	ODPB4	0: Disable PB4 open-drain 1: Enable PB4 open-drain
5	ODPB5	0: Disable PB5 open-drain 1: Enable PB5 open-drain
7~6	--	Reserved, Read as “0”

(14) TMR1：R50

(15) PR1 (Period Register)：R51
Timer 1 Period Register

(16) Duty_Cycle1 (Duty Cycle Register)：R52
Timer 1 Duty Cycle 1 Register

(17) T1CON：R53

Bit	Symbol	Function	
		Bit value	TIMER 1 rate
2~0	PS2~0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	1 : 1 1 : 4 1 : 8 1 : 16 1 : 32 1 : 64 1 : 128 1 : 256
3	TM2_ON	0：TIMER 1 OFF 1：TIMER 1 ON	
4-6	CHS2:0	PWM period pin select (PB0,1,2,4,5) 000：PB0 001：PB1 010：PB2 011：PB4 100：PB5	
7	T1IF	Time1 and PR1compare interrupt flag 1：Timer1and PR1 compare (must be cleared in software) 0：Timer1and PR1 not compare	

(18)Duty_Cycle2 (Duty Cycle Register)：R54
Timer 1 Duty Cycle 2 Register

(19)CHSA ：R55

Bit	Symbol	Function
2~0	CHSA2:0	PWM period pin select (PA0,1,2,3,4,5) 000：PA0 001：PA1 010：PA2 011：PA3 100：PA4 101：PA5
3	DC2ON	Duty_Cycle 2 duty cycle on/off 1：Enable 0：disable
4-5	PWM1LSB0 PWM1LSB1	These bit are the two PWM LSB of PWM duty cycle.(PWM1 use)
6-7	PWM2LSB0 PWM2LSB1	These bit are the two PWM LSB of PWM duty cycle.(PWM2 use)

(20) TMR (Time Mode Register): R81

Bit	Symbol	Function		
2~0	PS2~0	Prescaler Value	RTCC rate	WDT rate
		0 0 0	1 : 2	1 : 1
		0 0 1	1 : 4	1 : 2
		0 1 0	1 : 8	1 : 4
		0 1 1	1 : 16	1 : 8
		1 0 0	1 : 32	1 : 16
		1 0 1	1 : 64	1 : 32
		1 1 0	1 : 128	1 : 64
		1 1 1	1 : 256	1 : 128
3	PSC	Prescaler assignment bit: 0: RTCC 1: Watchdog Timer		
4	TCE	RTCC signal Edge: 0: Increment on low-to-high transition on RTCC pin 1: Increment on high-to-low transition on RTCC pin		
5	TCS	RTCC signal set: 0: Internal instruction cycle clock 1: Transition on RTCC pin		
6	IES	Interrupt edge select: 0: interrupt on falling edge on PB0 1: interrupt on rising edge on PB0		
7	--	Reserved, Read as “0”		

(21) CPIO A (Control Port I/O Mode Register): R85
＝“0”, I/O pin in output mode;
＝“1”, I/O pin in input mode.

(22) CPIO B (Control Port I/O Mode Register): R86
＝“0”, I/O pin in output mode;

＝“1”, I/O pin in input mode.

(23) PSTA: R87

Bit	Symbol	Function
0	--	Reserved, Read as “0”
1	PORB	0: Power on Reset occurred. 1: No Power on Reset occurred.
7~2	--	Reserved, Read as “0”

(24) PAIE: R88

Bit	Symbol	Function
0	PA0IE	0: Disable PA0 pin change interrupt 1: Enable PA0 pin change interrupt
1	PA1IE	0: Disable PA1 pin change interrupt 1: Enable PA1 pin change interrupt
2	PA2IE	0: Disable PA2 pin change interrupt 1: Enable PA2 pin change interrupt
3	PA3IE	0: Disable PA3 pin change interrupt 1: Enable PA3 pin change interrupt
4	PA4IE	0: Disable PA4 pin change interrupt 1: Enable PA4 pin change interrupt
5	PA5IE	0: Disable PA5 pin change interrupt 1: Enable PA5 pin change interrupt
7~6	--	Reserved, Read as “0”

(25) PAIF: R89

Bit	Symbol	Function
0	PA0IF	0: No PA0 pin change interrupt occurred 1: The PA0 pin change interrupt occurred
1	PA1IF	0: No PA1 pin change interrupt occurred 1: The PA1 pin change interrupt occurred
2	PA2IF	0: No PA2 pin change interrupt occurred 1: The PA2 pin change interrupt occurred
3	PA3IF	0: No PA3 pin change interrupt occurred 1: The PA3 pin change interrupt occurred
4	PA4IF	0: No PA4 pin change interrupt occurred 1: The PA4 pin change interrupt occurred
5	PA5IF	0: No PA5 pin change interrupt occurred 1: The PA5 pin change interrupt occurred
7~6	--	Reserved, Read as “0”

(26) /PHPA: R8C

Bit	Symbol	Function
0	/PHPA0	0: Enable PA0 internal pull-high 1: Disable PA0 internal pull-high
1	/PHPA1	0: Enable PA1 internal pull-high 1: Disable PA1 internal pull-high
2	/PHPA2	0: Enable PA2 internal pull-high 1: Disable PA2 internal pull-high
3	/PHPA3	0: Enable PA3 internal pull-high 1: Disable PA3 internal pull-high
4	/PHPA4	0: Enable PA4 internal pull-high 1: Disable PA4 internal pull-high
5	/PHPA5	0: Enable PA5 internal pull-high 1: Disable PA5 internal pull-high
7~6	--	Reserved, Read as “0”

(27) /PLPA: R8D

Bit	Symbol	Function
0	/PLPA0	0: Enable PA0 internal pull-low 1: Disable PA0 internal pull-low
1	/PLPA1	0: Enable PA1 internal pull-low 1: Disable PA1 internal pull-low
2	/PLPA2	0: Enable PA2 internal pull-low 1: Disable PA2 internal pull-low
3	/PLPA3	0: Enable PA3 internal pull-low 1: Disable PA3 internal pull-low
4	/PLPA4	0: Enable PA4 internal pull-low 1: Disable PA4 internal pull-low
5	/PLPA5	0: Enable PA5 internal pull-low 1: Disable PA5 internal pull-low
7~6	--	Reserved, Read as “0”

(28) ODPA: R8E

Bit	Symbol	Function
0	ODPA0	0: Disable PA0 open-drain 1: Enable PA0 open-drain
1	ODPA1	0: Disable PA1 open-drain 1: Enable PA1 open-drain
2	ODPA2	0: Disable PA2 open-drain 1: Enable PA2 open-drain
3	ODPA3	0: Disable PA3 open-drain 1: Enable PA3 open-drain
4	ODPA4	0: Disable PA4 open-drain 1: Enable PA4 open-drain

Bit	Symbol	Function
5	ODPA5	0: Disable PA5 open-drain 1: Enable PA5 open-drain
7~6	--	Reserved, Read as “0”

(29) Configurable options for EPROM (Set by writer):

Type	Option
INRC Oscillator	8MHz
	4MHz
Watchdog Timer control	Watchdog timer disable all the time
	Watchdog timer enable all the time
Oscillator-start Timer Control	0ms
	75ms
Security state	Security Disable
	Security Enable

(B) Program Memory

Address	Description
000-3FF	Program memory
000	The starting address of power on or WDT time-out reset.
004	Interrupt vector

7. Reset Condition for all Registers

Register	Address	Power-On Reset	/MCLR or WDT Reset	Wake-up from SLEEP
IAR	00h	—	—	—
RTCC	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PC	02h	00 0000 0000	00 0000 0000	PC+1
STATUS	03h	0001 1xxx	000# #uuu	000# #uuu
MSR	04h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORT A	05h	--xx xxxx	--uu uuuu	--uu uuuu
PORT B	06h	--xx xxxx	--uu uuuu	--uu uuuu
PBIE	08h	--00 0000	--00 0000	--uu uuuu
PBIF	09h	--xx xxxx	--uu uuuu	--uu uuuu
PCHLAT	0Ah	---- --00	---- --00	---- --uu

Register	Address	Power-On Reset	/MCLR or WDT Reset	Wake-up from SLEEP
INTS	0Bh	0-00 -00-	0-00 -00-	u-uu -uu-
/PHPB	0Ch	--11 -111	--11 -111	--uu -uuu
/PLPB	0Dh	--11 -111	--11 -111	--uu -uuu
ODPB	0Eh	--00 -000	--00 -000	--uu -uuu
TMR1	50h	0000 0000	0000 0000	uuuu uuuu
PR1	51h	1111 1111	1111 1111	uuuu uuuu
Duty cycle1	52h	0000 0000	0000 0000	uuuu uuuu
T1CON	53h	-000 0000	-000 0000	-uuu uuuu
Duty cycle2	54h	0000 0000	0000 0000	uuuu uuuu
CHSA	55h	0000 0000	0000 0000	uuuu uuuu
TMR	81h	1111 1111	1111 1111	uuuu uuuu
CPIO A	85h	--11 1111	--111 1111	--11 1111
CPIO B	86h	--11 1111	--11 1111	--11 1111
PSTA	87h	---- --q-	---- --u-	---- --q-
RAIE	88h	--00 0000	--00 0000	--uu uuuu
RAIF	89h	--xx xxxx	--uu uuuu	--uu uuuu
/PHPA	8Ch	--11 1111	--11 1111	--uu uuuu
/PLPA	8Dh	--11 1111	--11 1111	--uu uuuu
ODPA	8Eh	--00 0000	--00 0000	--uu uuuu

Note: u =unchanged, x =unknown, - =unimplemented, read as “0”

=value depends on the condition of the following table

Condition	PC	Status: bit 4	Status: bit 3	Status: bit 1	Status: bit 0
WDT reset (not during SLEEP)	000h	0	1	u	u
WDT reset during SLEEP	PC+1	0	0	u	u
Power on reset	000h	1	1	x	x
interrupt wake_up from sleep	PC+1	1	0	u	u

For 10P611			
INT_RC	Power_up		Wake_up from sleep
4M/8M	PWRT=1	PWRT=0	- -
	72ms+1024Tosc	1024Tosc	1024 Tosc

8. Instruction Set :

Instruction Code	Mnemonic Operands	Function	Operating	Status
010000 00000000	NOP	No operation	None	
010000 00000001	CLRWT	Clear Watchdog timer	0→WT	TF, PF
010000 00000010	SLEEP	Sleep mode	0→WT, stop OSC	TF, PF
010000 00000011	TMODE	Load W to TMODE register	W→TMODE	None
010000 00000100	RET	Return	Stack→PC	None
010000 00000rrr	CPIO R	Control I/O port register	W→CPIO r	None
010001 1rrrrrrr	STWR R	Store W to register	W→R	None
011000 trrrrrrr	LDR R, t	Load register	R→t	Z
111010 iiiiiiii	LDWI i	Load immediate to W	I→W	None
010111 trrrrrrr	SWAPR R, t	Swap halves register	[R(0~3) ↔R(4~7)]→t	None
011001 trrrrrrr	INCR R, t	Increment register	R + 1→t	Z
011010 trrrrrrr	INCRSZ R, t	Increment register, skip if zero	R + 1→t	None
011011 trrrrrrr	ADDWR R, t	Add W and register	W + R→t	C, HC, Z
011100 trrrrrrr	SUBWR R, t	Subtract W from register	R – W→t or (R+/W+1→t)	C, HC, Z
011101 trrrrrrr	DECR R, t	Decrement register	R – 1→t	Z
011110 trrrrrrr	DECRSZ R, t	Decrement register, skip if zero	R – 1→t	None
010010 trrrrrrr	ANDWR R, t	AND W and register	R ∩ W→t	Z
110100 iiiiiiii	ANDWI i	AND W and immediate	i ∩ W→W	Z
010011 trrrrrrr	IORWR R, t	Inclu. OR W and register	R ∪ W→t	Z
110101 iiiiiiii	IORWI i	Inclu. OR W and immediate	i ∪ W→W	Z
010100 trrrrrrr	XORWR R, t	Exclu. OR W and register	R ⊕ W→t	Z
110110 iiiiiiii	XORWI i	Exclu. OR W and immediate	i ⊕ W→W	Z
011111 trrrrrrr	COMR R, t	Complement register	/R→t	Z
010110 trrrrrrr	RRR R, t	Rotate right register	R(n) →R(n-1), C→R(7), R(0)→C	C
010101 trrrrrrr	RLR R, t	Rotate left register	R(n)→r(n+1), C→R(0), R(7)→C	C
010000 1xxxxxxx	CLRW	Clear working register	0→W	Z
010001 0rrrrrrr	CLRR R	Clear register	0→R	Z
0000bb brrrrrrr	BCR R, b	Bit clear	0→R(b)	None
0010bb brrrrrrr	BSR R, b	Bit set	1→R(b)	None
0001bb brrrrrrr	BTSC R, b	Bit Test, skip if clear	Skip if R(b)=0	None
0011bb brrrrrrr	BTSS R, b	Bit Test, skip if set	Skip if R(b)=1	None
1000nn nnnnnnnn	LCALL n	Long CALL subroutine	n→PC, PC+1→Stack	None

Instruction Code	Mnemonic Operands	Function	Operating	Status
1010nn nnnnnnnn	LJUMP n	Long JUMP to address	n→PC	None
110111 iiiiiiii	ADDWI	Add immediate to W	W+i→W	C,HC,Z
110001 iiiiiiii	RTWI i	Return, place immediate to W	Stack→PC,i→W	None
111000 iiiiiiii	SUBWI	Subtract W from immediate	I-W→W	C,HC,Z
010000 00001001	RTFI	Return from interrupt	Stack→PC,1→GIS	None

Note :

W	:	Working register	b	:	Bit position
WT	:	Watchdog timer	t	:	Target
TMODE	:	TMODE mode register		0	: Working register
CPIO	:	Control I/O port register		1	: General register
TF	:	Timer overflow flag	R	:	General register address
PF	:	Power loss flag	C	:	Carry flag
PC	:	Program Counter	HC	:	Half carry
OSC	:	Oscillator	Z	:	Zero flag
Inclu.	:	Inclusive '∪'	/	:	Complement
Exclu.	:	Exclusive '⊕'	x	:	Don't care
AND	:	Logic AND '∩'	i	:	Immediate data (8 bits)
			n	:	Immediate address

9.Electrical characteristics

1.Operation Current :

(1)INT_RC,WDT – enable ，內建 4Mhz，PED=disable 1.8V，PUT=75ms

IC1：

	Freq.	Current	Sleep
2.1V	4.148M	178uA	1.7uA
3.0V	4.095M	266uA	3.6uA
4.0V	3.99M	403uA	7uA
5.0V	3.956M	563uA	11uA
5.5V	3.952M	650uA	14.5uA
6V	3.958M	758uA	16.2uA

IC2：

	Freq.	Current	Sleep
2.1V	4.148M	178uA	1.7uA
3.0V	4.095M	266uA	3.6uA
4.0V	3.99M	403uA	7uA
5.0V	4.08M	607uA	11uA
5.5V	3.952M	650uA	14.5uA
6V	3.958M	758uA	16.2uA

(2)INT_RC,WDT – enable ，內建 8Mhz，PED=disable 1.8V，PUT=75ms

IC1:

	Freq.	Current	Sleep
2.1V	8.5M	261uA	1uA
3.0V	8.248M	416uA	4uA
4.0V	8.042M	631uA	10uA
5.0V	7.928M	847uA	17uA
5.5V	7.912M	988uA	22uA
6V	7.9M	1.1mA	27uA

2. Input Voltage (Vdd = 5V) :

(1) TTL input buffer :

	PB	PA
Vt	1.4V	1.4V

(2) Schmitt trigger (Vdd = 5V) :

	Vil	Vih
RTCC	1.1	2.8V

3. Output Voltage (Vdd = 5V) :

	PB	PA	Condition
Voh	4.1V	4.1V	-5mA
Vol	0.4V	0.4V	8mA
Voh	*	*	-5mA
Vol	*	*	5mA

4. Output Current (Max.) (Vdd = 5V) :

PortA,B:

	PB	PC
soure current	15mA	15mA
sink current	30mA	30mA

5. The basic WDT time-out cycle time :

	IC1
2.3V	27.5
3.0V	23.5
4.0V	21
5.0V	19.5
6.3V	18

Unit = ms

6. PED Voltage:

	IC1	IC2	
PED	1.9V	2.0V	PED=1.8V 準位

7.Internal pull_up & Pull_down：

	Pull_up	Pull_down
PA	115K	131K
PB	115K	130K